

1 CLAIMS:

2 1. A method of forming a capacitor comprising the following
3 steps:

4 forming a mass of silicon material over a node location, the mass
5 comprising two forms of silicon;

6 substantially selectively forming rugged polysilicon from one of the
7 forms of silicon and not from the other of the forms of silicon; and

8 forming a capacitor dielectric layer and a complementary capacitor
9 plate proximate the rugged polysilicon.

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11 2. The method of claim 1 wherein the two forms of silicon
12 comprise doped silicon and undoped silicon.

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14 3. The method of claim 2 wherein the doped silicon comprises
15 a dopant concentration of at least 5×10^{18} atoms/cm³ and wherein the
16 undoped silicon comprises a dopant concentration of less than 5×10^{18}
17 atoms/cm³.

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19 4. The method of claim 2 wherein the doped silicon comprises
20 a dopant concentration of at least 1×10^{19} atoms/cm³ and wherein the
21 undoped silicon comprises a dopant concentration of less than or equal
22 to 1×10^{18} atoms/cm³.

1 5. A method of forming a capacitor comprising the following
2 steps:

3 forming a mass of silicon material over a node location, the mass
4 comprising exposed doped silicon and exposed undoped silicon;

5 substantially selectively forming rugged polysilicon from the exposed
6 undoped silicon and not from the exposed doped silicon; and

7 forming a capacitor dielectric layer and a complementary capacitor
8 plate proximate the rugged polysilicon and doped silicon.

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10 6. The method of claim 5 wherein the step of forming a mass
11 of silicon material comprises forming a layer of doped silicon between
12 two layers of undoped silicon.

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14 7. The method of claim 5 further comprising conductively
15 doping the undoped silicon after forming the rugged polysilicon.

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17 8. The method of claim 5 further comprising, after forming the
18 rugged polysilicon, out-diffusing impurity from the doped silicon into the
19 undoped silicon to conductively dope the undoped silicon.

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21 9. The method of claim 5 wherein the step of forming the
22 mass comprises forming the exposed undoped silicon to be substantially
23 amorphous.

1 10. The method of claim 5 wherein the step of forming the
2 mass comprises forming the exposed doped silicon to be substantially
3 polycrystalline.

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5 11. A method of forming a capacitor comprising the following
6 steps:

7 forming an insulative layer over a node location;

8 forming an opening through the insulative layer to the node
9 location;

10 forming two forms of silicon within the opening, the two forms
11 of silicon together forming a capacitor storage node;

12 exposing the two forms of silicon to common subsequent
13 processing conditions which substantially selectively forming rugged
14 polysilicon from one of the exposed two forms of silicon and not from
15 the other of the exposed two forms of silicon;

16 forming a dielectric layer proximate the storage node; and

17 forming a cell plate layer proximate the dielectric layer.

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19 12. The method of claim 11 wherein the two forms of silicon
20 comprise doped silicon and undoped silicon.

1 13. A method of forming a capacitor comprising the following
2 steps:

3 forming an insulative layer over a node location:

4 forming an opening through the insulative layer to the node
5 location;

6 forming silicon material within the opening, the silicon material
7 comprising doped silicon and undoped silicon and defining a capacitor
8 storage node;

9 removing a portion of the insulative layer to expose a sidewall
10 surface of the storage node, the exposed sidewall surface comprising
11 undoped silicon;

12 forming HSG from the undoped silicon of the exposed sidewall
13 surface;

14 forming a capacitor dielectric layer proximate the storage node;
15 and

16 forming a complementary capacitor plate proximate the capacitor
17 dielectric layer.

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19 14. The method of claim 13 wherein the doped silicon comprises
20 polysilicon and the undoped silicon comprises substantially amorphous
21 silicon.
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1 15. The method of claim 13 wherein the step of forming the
2 silicon material comprises forming a layer of doped silicon between two
3 layers of undoped silicon.

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5 16. The method of claim 13 wherein the step of forming the
6 silicon material comprises forming a layer of doped polysilicon between
7 two layers of undoped substantially amorphous silicon.

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9 17. A method of forming a capacitor comprising the following
10 steps:

11 forming an insulative layer over a node location;

12 forming an opening through the insulative layer to the node
13 location;

14 forming an undoped silicon layer within the opening to narrow the
15 opening;

16 forming a doped silicon layer within the narrowed opening, the
17 undoped silicon layer and doped silicon layer together defining a
18 capacitor storage node;

19 forming a capacitor dielectric layer proximate the storage node;
20 and

21 forming a complementary capacitor plate proximate the capacitor
22 dielectric layer.

1 18. The method of claim 17 wherein the undoped silicon layer
2 comprises substantially amorphous silicon.

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4 19. The method of claim 17 wherein the doped silicon layer
5 comprises polysilicon.

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7 20. The method of claim 17 further comprising:
8 removing a portion of the insulative layer to expose a sidewall
9 surface of the storage node comprising the undoped silicon layer; and
10 forming rugged polysilicon from the exposed sidewall surface.

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12 21. The method of claim 17 further comprising:
13 exposing a surface of the capacitor storage node comprising
14 undoped silicon;

15 exposing a surface of the capacitor storage node comprising doped
16 silicon; and

17 substantially selectively forming HSG polysilicon from the exposed
18 capacitor storage node surface comprising undoped silicon and not from
19 the exposed capacitor storage node surface comprising doped silicon.
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1 22. The method of claim 21 wherein the formation of the
2 rugged polysilicon comprises:

3 *in situ* HF cleaning of the exposed sidewall surface;
4 seeding the exposed sidewall surface with polysilicon; and
5 annealing the seeded sidewall surface at about 560° C for
6 about 20 minutes.

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8 23. The method of claim 21 wherein the formation of the
9 rugged polysilicon comprises:

10 *in situ* HF cleaning of the exposed sidewall surface;
11 seeding the exposed sidewall surface with polysilicon;
12 annealing the seeded sidewall surface at about 560° C for
13 about 20 minutes; and
14 a polysilicon etch after the annealing to remove any monolayers
15 of silicon.

1 24. A method of forming a capacitor comprising the following
2 steps:

3 forming an insulative layer over a node location;

4 forming an opening through the insulative layer to the node
5 location;

6 forming a first undoped silicon layer within the opening to narrow
7 the opening;

8 forming a doped silicon layer within the narrowed opening to
9 further narrow the opening;

10 forming a second undoped silicon layer within the further
11 narrowed opening; the first undoped silicon layer, second undoped silicon
12 layer and doped silicon layer together defining a capacitor storage node;

13 removing a portion of the insulative layer to expose a sidewall
14 surface of the storage node comprising the first undoped silicon layer;

15 forming rugged polysilicon on the exposed sidewall surface;

16 forming a dielectric layer proximate the storage node; and

17 forming a cell plate layer proximate the dielectric layer.
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1 25. The method of claim 24 further comprising:

2 exposing a surface of the capacitor storage node comprising the
3 second undoped silicon layer;

4 exposing a surface of the capacitor storage node comprising the
5 doped silicon layer; and

6 substantially selectively forming HSG polysilicon from the exposed
7 capacitor storage node surface comprising undoped silicon and not from
8 the exposed capacitor storage node surface comprising doped silicon.

9
10 26. A method of forming a DRAM array comprising the
11 following steps:

12 defining a first node location, a second node location and a third
13 node location; the second node location being electrically coupled to the
14 first node location through a first transistor gate; the second node
15 location being electrically coupled to the third node location through a
16 second transistor gate;

17 forming an electrically insulative layer over the node locations;

18 removing portions of the electrically insulative layer to form a
19 first opening, a second opening, and a third opening; the first, second
20 and third openings extending to the first, second and third node
21 locations, respectively;

22 forming an undoped silicon layer within the first, second and third
23 openings to narrow the first, second and third openings;

forming a doped silicon layer within the narrowed openings; the undoped silicon layer and the doped silicon layer within the first opening together defining a first storage node; the undoped silicon layer and the doped silicon layer within the third opening together defining a second storage node; the undoped silicon layer and the doped silicon layer within the second opening together defining a conductive contact;

removing a portion of the electrically insulative layer to expose sidewall surfaces of the first storage node, the second storage node and the conductive contact;

forming rugged polysilicon on the exposed sidewall surfaces;

forming a dielectric layer proximate the first and second storage nodes;

forming a cell plate layer proximate the dielectric layer; the cell plate layer, dielectric layer and first storage node together defining a first capacitor; the cell plate layer, dielectric layer and second storage node together defining a second capacitor; and

forming a bitline electrically connected to the conductive contact; the conductive contact and first capacitor together defining a first DRAM cell; the conductive contact and second capacitor together defining a second DRAM.

1 27. The method of claim 26 wherein the exposed sidewall
2 surfaces comprise undoped silicon, the method further comprising:

3 exposing a surface of the first storage node comprising the doped
4 silicon layer;

5 exposing a surface of the second storage node comprising the
6 doped silicon layer; and

7 substantially selectively forming HSG polysilicon from the exposed
8 first and second storage node surfaces comprising undoped silicon and
9 not from the exposed first and second storage node surfaces comprising
10 doped silicon.

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12 28. The method of claim 26 wherein the doped and undoped
13 silicon layers are formed over the insulative layer, the method further
14 comprising polishing the doped and undoped silicon layers to remove
15 the doped and undoped silicon layers from over the electrically
16 insulative layer.

1 29. A method of forming a DRAM array comprising the
2 following steps:

3 defining a first node location, a second node location and a third
4 node location; the second node location being electrically coupled to the
5 first node location through a first transistor gate; the second node being
6 electrically coupled to the third node location through a second
7 transistor gate;

8 forming an electrically insulative layer over the node locations;

9 removing portions of the electrically insulative layer to form a
10 first opening, a second opening, and a third opening; the first, second
11 and third openings extending to the first, second and third node
12 locations, respectively;

13 forming an undoped silicon layer within the first, second and third
14 openings to narrow the first, second and third openings;

15 forming a doped silicon layer within the narrowed first, second
16 and third openings to further narrow the first, second and third
17 openings;

18 forming a second undoped silicon layer within the further
19 narrowed first, second and third openings; the first undoped silicon
20 layer, second undoped silicon layer and doped silicon layer within the
21 first opening together defining a first storage node; the first undoped
22 silicon layer, second undoped silicon layer and doped silicon layer within
23 the third opening together defining a second storage node; the first
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1 undoped silicon layer, second undoped silicon layer and doped silicon
2 layer within the second opening together defining a conductive contact;
3 removing a portion of the electrically insulative layer to expose
4 sidewall surfaces of the first and second storage nodes and of the
5 conductive contact;
6 forming rugged polysilicon on the exposed sidewall surfaces;
7 forming a dielectric layer proximate the first and second storage
8 nodes;
9 forming a cell plate layer proximate the dielectric layer; the cell
10 plate layer, dielectric layer and first storage node together defining a
11 first capacitor; the cell plate layer, dielectric layer and second storage
12 node together defining a second capacitor; and
13 forming a bitline electrically connected to the conductive contact;
14 the conductive contact and first capacitor together defining a first
15 DRAM cell; and the conductive contact and second capacitor together
16 defining a second DRAM cell.

1 30. The method of claim 29 wherein the exposed sidewall
2 surfaces comprise the first undoped silicon layer, the method further
3 comprising:

4 exposing a surface of the first storage node comprising the second
5 undoped silicon layer;

6 exposing a surface of the first storage node comprising the doped
7 silicon layer;

8 exposing a surface of the second storage node comprising the
9 second undoped silicon layer;

10 exposing a surface of the second storage node comprising the
11 doped silicon layer; and

12 substantially selectively forming HSG polysilicon over the exposed
13 first and second storage node surfaces comprising undoped silicon and
14 not over the exposed first and second storage node surfaces comprising
15 doped silicon.

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17 31. The method of claim 29 wherein the doped and undoped
18 silicon layers are formed over the insulative layer, the method further
19 comprising polishing the doped and undoped silicon layers to remove
20 the doped and undoped silicon layers from over the electrically
21 insulative layer.

1 32. A method of forming a monolithic integrated circuit
2 comprising the following steps:

3 fabricating integrated circuitry over a portion of a semiconductor
4 substrate, the integrated circuitry comprising elements including
5 transistors, capacitors and resistive elements;

6 the fabrication of at least one of the capacitors comprising the
7 following steps:

8 forming a mass of silicon material over a node location, the
9 mass comprising exposed doped silicon and exposed undoped
10 silicon;

11 substantially selectively forming rugged polysilicon from the
12 exposed undoped silicon and not from the exposed doped silicon;
13 and

14 forming a capacitor dielectric layer and complementary
15 capacitor plate proximate the rugged polysilicon and doped
16 silicon.

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18 33. The method of claim 32 wherein the monolithic integrated
19 circuit is fabricated as part of a microprocessor circuit.

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21 34. The method of claim 32 wherein the monolithic integrated
22 circuit is fabricated as part of a microprocessor circuit and wherein the
23 capacitor is integrated into a DRAM cell.
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1 35. A capacitor comprising:
2 a first capacitor plate;
3 a second capacitor plate;
4 a capacitor dielectric layer intermediate the first and second
5 capacitor plates; and

6 at least one of the first and second capacitor plates comprising
7 a surface against the capacitor dielectric layer and wherein said surface
8 comprises both doped rugged polysilicon and doped non-rugged
9 polysilicon.

10
11 36. A capacitor comprising:
12 a capacitor storage node having a rugged-polysilicon-comprising
13 lateral surface and a top surface, a predominate portion of the top
14 surface not comprising rugged polysilicon;

15 a dielectric layer proximate the capacitor storage node; and
16 a cell plate layer proximate the dielectric layer.

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18 37. The capacitor of claim 36 wherein the storage node further
19 comprises a container shape and an interior rugged-polysilicon-comprising
20 surface.

1 38. A DRAM array comprising:
2 a first node location, a second node location and a third node
3 location associated with a semiconductor substrate;
4 a first transistor gate electrically coupling the first node location
5 to the second storage node location;
6 a second transistor gate electrically coupling the third node
7 location to the second node location;
8 an electrically insulative layer over the node locations;
9 a first storage node extending through the electrically insulative
10 layer to the first node location, the first storage node having a rugged-
11 polysilicon-comprising lateral surface and top surface, a predominate
12 portion of the top surface not comprising rugged polysilicon;
13 a second storage node extending through the electrically insulative
14 layer to the third node location, the second storage node having a
15 rugged-polysilicon-comprising lateral surface and a top surface, a
16 predominate portion of the top surface not comprising rugged
17 polysilicon;
18 a conductive contact extending through the electrically insulative
19 layer to the second node location;
20 a first dielectric layer proximate the first storage node;
21 a first cell plate layer proximate the first dielectric layer; the first
22 cell plate layer, first dielectric layer and first storage node together
23 defining a first capacitor;
24 a second dielectric layer proximate the second storage node;

1 a second cell plate layer proximate the second dielectric layer; the
2 second cell plate layer, second dielectric layer and second storage node
3 together defining a second capacitor; and

4 a bitline electrically connected to the conductive contact; the
5 conductive contact and first capacitor together defining a first DRAM
6 cell electrically connected to the bitline; the conductive contact and
7 second capacitor together defining a second DRAM cell electrically
8 connected to the bitline.

9
10 39. The DRAM array of claim 38 wherein the conductive
11 contact has a rugged-polysilicon-comprising lateral surface.

12
13 40. The DRAM array of claim 38 wherein the first and second
14 capacitor storage nodes comprise container shapes and further include
15 interior rugged-polysilicon-comprising surfaces.

1 41. A monolithic integrated circuit comprising:
2 fabricated circuitry over a semiconductor substrate, the integrated
3 circuitry comprising elements including transistors, capacitors and resistive
4 elements;

5 at least one of the capacitors comprising:

6 a first capacitor plate;

7 a second capacitor plate;

8 a capacitor dielectric layer intermediate the first and second
9 capacitor plates; and

10 at least one of the first and second capacitor plates
11 comprising a surface against the capacitor dielectric layer and
12 wherein said surface comprises both doped rugged polysilicon and
13 doped non-rugged polysilicon.

14
15 42. The monolithic integrated circuit of claim 41 wherein the
16 monolithic integrated circuit is part of a microprocessor circuit.

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18 43. The monolithic integrated circuit of claim 41 wherein the
19 monolithic integrated circuit is part of a microprocessor circuit and
20 wherein the at least one capacitor is incorporated into a DRAM cell.
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